UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,909	01/08/2007	Noritaka Muraki	Q79714	1815

23373 7590 02/12/2008

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
HUBER, ROBERT T	
ART UNIT	PAPER NUMBER
4146	
MAIL DATE	DELIVERY MODE
02/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,909	MURAKI ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	4146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2006 and 04 October 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/24/2006, 01/08/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the well layer containing a thick portion having a large thickness and a thin portion having a small thickness, as claimed in claim 1, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3 – 5, 11, 16, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (US 6,608,330 B1).

a. Regarding claim 1, Yamada discloses a gallium nitride compound semiconductor light-emitting device (e.g. figure 1) comprising

a crystalline substrate (substrate 101);

a light-emitting of a quantum well structure layer (active layer 106) which is formed of a gallium nitride compound semiconductor barrier layer (layers 107) and a gallium nitride compound semiconductor well layer (layers 108 and 109), which light-emitting layer is provided on a second side of the crystalline substrate (e.g. as seen in figure 1);

a contact layer formed of a Group III-V compound semiconductor for providing an Ohmic electrode for supplying device operation current to the light-emitting layer (layer 111, formed from GaN as stated in col. 8, line 41); and

an Ohmic electrode (electrode 112)) which is provided on the contact layer (e.g. as seen in figure 1) and has an aperture through which a portion of the contact layer is exposed (e.g. as seen in figure 1, the sides of electrode 112 are open, exposing the contact layer 111),

wherein the Ohmic electrode exhibits light permeability with respect to light emitted from the light-emitting layer (col. 10, line 42 discloses the electrode 112 to be transparent), and the well layer contains a thick portion having a large thickness and a thin portion having a small thickness (e.g. col. 13, lines 16 - 36, with reference to figure 6, disclose that the well layers have both thin and thick regions).

b. Regarding claim 2, Yamada discloses a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, wherein the well layer contains a portion having a thickness of 1.5 nm to 0 nm (col. 13, lines 20 – 22 disclose that, with reference to figure 6, disclose that the well layers have regions with thickness less than half of the average thickness. Col. 9, lines 35 - 36 disclose the average thickness of a well layer to be 3 nm. Therefore, the regions defined by "D" in figure 6 of the well layers are less than 1.5 nm).

c. Regarding claims 3 - 5, Yamada discloses a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above. Yamada further discloses the predetermined impurity element added only to the barrier layer is silicon (e.g. col. 10, lines 3 – 7, discloses that either the well layer or the barrier layer may be doped with Silicon).

d. Regarding claim 11, Yamada discloses a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, wherein the Ohmic electrode has a thickness of 1 nm to 100 nm (col. 10, lines 42 – 43, disclose the electrode has a thickness of 20 nm).

e. Regarding claims 16 and 17, Yamada discloses a lamp and an LED employing the gallium nitride compound semiconductor light- emitting device according to claim 1 (col. 11, lines 25 – 36).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Hanaoka et al. (US 5,804,839).

a. Regarding claim 6, Yamada discloses a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above. However, Yamada is silent with respect to the contact layer being doped with an n- type impurity element and has a carrier concentration of 5×10^{18} cm^{-3} to 2×10^{19} cm^{-3}. Hanaoka teaches that GaN layers may be formed with n-type impurity concentrations of 1×10^{19} cm^{-3} (col. 9, lines 20 - 23).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the contact layer of Yamada to include n-type impurities with a concentration of 1 x 10^{19} cm^{-3} since Hanaoka discloses that this is known structure used for light emitting devices. One would have been motivated to make such a modification since it would allow the layer to exhibit light transmission properties, allowing the light to transmit readily through the layer, and desirable electrical properties for tuning the light emitting device.

b. Regarding claims 7 and 8, Yamada discloses a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, wherein the contact layer is doped with a p - type impurity element (col. 8, line 41). Yamada is silent with respect to the layer having a carrier concentration of 1 x 10^{17} cm^{-3} to 1 x 10^{18} cm^{-3}. Hanaoka teaches that p-type contact layers may be doped with a carrier concentration of 1 x 10^{18} cm^{-3} (col. 3, lines 48 – 49).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the contact layer of Yamada to have a p-type impurity concentration of 1 x 10^{18} cm^{-3} since Hanaoka discloses that this is known contact layer structure used in light emitting devices. One would have been motivated to make such a modification since it would allow the layer to exhibit light transmission properties, allowing the light to transmit readily through the layer, and desirable electrical properties for tuning the light emitting device.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada. Yamada discloses a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, however Yamada is silent with respect to the contact layer having a thickness of 1 μm to 3 μm. Yamada discloses that the contact layer thickness is 0.25 μm.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to enlarge the layer thickness of Yamada, since it has been held by the courts that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device, and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. *In Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984). One would be motivated to make such a modification of the layer thickness in order to make the device structurally more rigid.

7. Claims 12, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Morita et al. (US 6,121,636). Yamada discloses a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, however Yamada is silent with respect to a multilayered metallic reflecting mirror made of the same material identical to the Ohmic electrode for reflecting light emitted from the light-emitting layer to the outside, which is provided on a first side of the crystalline substrate. Morita discloses a mirror on the outside first side of the

crystalline substrate (e.g. figure 1, reflecting layer 11) wherein the metallic reflecting mirror contains a metallic material identical to that contained in the Ohmic electrode (e.g. col. 4, lines 1 – 9, discloses that the layer may be made of gold, which is the same material as the electrode 9). Morita further discloses that the layers may be multilayered (col. 2, lines 21 - 25).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the light emitting device of Yamada to include the reflecting mirror, as taught by Morita, since Morita discloses that multilayer reflecting mirrors, made of the same material as the electrode, can be added to light emitting devices. One would be motivated to add a reflecting mirror on the second side of the substrate in order to prevent light escaping from the bottom of the device, thereby protecting underlying structures, as taught in Morita in col. 8, lines 33 - 44. One would be motivated to make the reflecting mirror multilayered to enhance it reflecting ability. One would further be motivated to make the mirror of the same material as that of the Ohmic electrode since it would require fewer materials for the production process.

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada in view of Kaneyama et al. (US 6,452,214 B2). Yamada discloses a gallium nitride compound semiconductor light-emitting device according to claim 1, as cited above, however Yamada is silent with respect to a metallic reflecting mirror containing a single-metal film or an alloy film formed from at least one member selected from the group

consisting of silver, platinum, rhodium and aluminum. Kaneyama teaches a metallic reflecting mirror formed from aluminum (col. 4, lines 32 - 35).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the light emitting device of Yamada to include the reflecting mirror, as taught by Kaneyama, since Kaneyama discloses that reflecting mirrors made of aluminum can be added to light emitting devices. One would be motivated to add an aluminum reflecting mirror on the second side of the substrate in order to prevent light escaping from the bottom of the device, thereby protecting underlying structures, and aluminum is a readily available material that is can be relatively easily deposited on substrates via known deposition methods (i.e. sputtering, evaporation, etc..)

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Saito et al. (US 6,121,634) discloses a Nitride Semiconductor Light Emitting Device and Its Manufacturing Methods

b. Udagawa (US 6,153,894) discloses a Group III Nitride Semiconductor Light Emitting Device

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is

(571)270-3899. The examiner can normally be reached on Monday - Thursday (8am - 5pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marvin Lateef can be reached on (571) 272-5026. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Huber/
Examiner, Art Unit 4146
February 1, 2008

/Marvin M. Lateef/

Supervisory Patent Examiner, Art Unit 4146